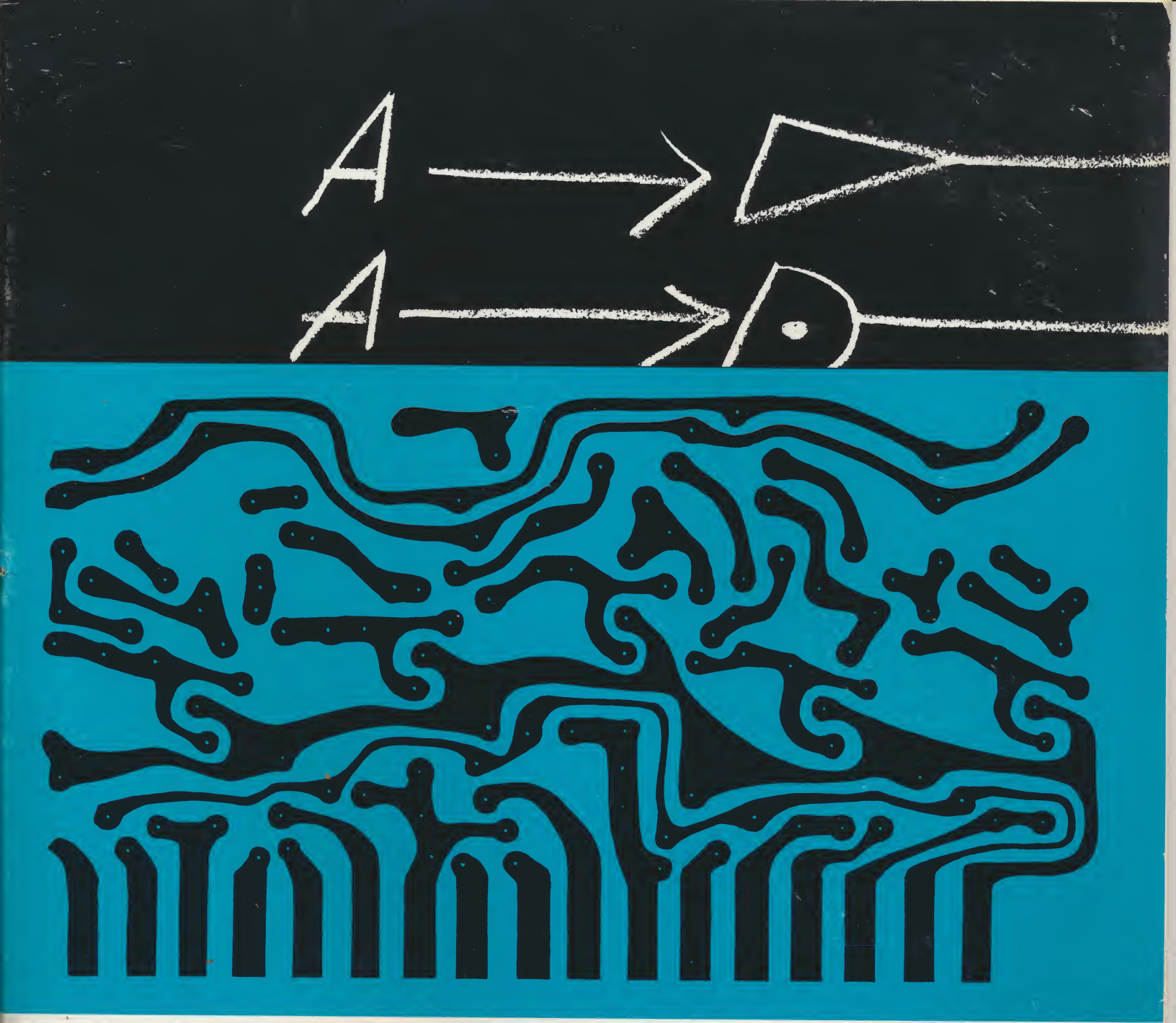


R-11

Microelectronic Computer

RAYTHEON COMPANY • MISSILE SYSTEMS DIVISION

TEST ERROR
PATT GEN
STOP ERROR
CLOCK STEP
CLOCK START
UNLD
LD
PAR ERROR
AC
MQ
FL
RA
XR
IOS
IOL
RC
LAMP TEST
LAC
LMQ
RESET
LT
SPM
STOP

introduction

The R-11 represents the latest in Raytheon's line of military computers. It follows in the footsteps of its predecessors by combining the most advanced design techniques with ultra reliable performance and reasonable cost and is designed with the system requirement parameter as the utmost consideration. It is thus ideal for tactical command and control; ground, airborne and naval data systems; fire control; communication switching; checkout; and scientific computation.

The R-11 combines integrated circuit design with standard components to achieve an MTBF in excess of 3500 hours. Basic design to meet MIL-E-5400 Cat. I specifications provides operation over the full temperature range of –54F to 160°F.

The entire computer is contained in three modular units: Arithmetic-Control Module, Memory Module, and Power Supply. The three units occupy 1.9 cubic feet, weigh 100 pounds, and provide 8,192 words of memory (24-bit word). Ease of maintenance has been given prime consideration by the adoption of only 19 circuit board types in a total of 79 boards. The basic software consists of documented packages ranging from machine diagnostics to symbolic assemblers. In addition, a full range of peripheral equipment is available with associated software.

Behind these characteristics lie the technical resources of one of the world's largest manufacturers of computers. Computers designed with the "system" in mind.

operational features

central data processor

The central data processor (CDP) is the heart of the R-11 computer system. It includes two functional areas; the arithmetic unit and program control. The arithmetic unit implements the add, subtract, multiply and divide instructions. The program control includes the memory addressing control, the interrupt control logic, and control logic for interfacing the CDP and I/O modules. There is no distinct separation between the arithmetic and control operation since many logic blocks are shared by the two functional units to increase overall efficiency.

memory

To meet various system and customer requirements, the basic memory has a storage capacity of 8192 words (each with 24 bits plus parity). It is expandable to 131,072 words of directly addressed memory in units of 4096 or 8192 words.

input/output channels

Asynchronous real-time input channels are capable of transferring 24-bit words at a word rate exceeding 1 MHz.

The program controlled I/O channel can transmit data at word rates greater than 250 kHz (24 bits) to and from 16 separate devices. Various program options are available to aid in the most efficient use of this channel. Among these are a high speed interrupt and test capability to allow interrogation of the status of the I/O control. The I/O instruction set provides sufficient flexibility for low as well as high speed applications.

power supply

The power supply for the R-11 is available in both 60 and 400 cycle models. Its design stresses reliability, efficiency and compactness, and it is a modular part of the 100 pound, 1.9 cubic foot computer package.

general characteristics

Type:	Digital, stored program, synchronous parallel, fixed point, fractional binary, two's complement, arithmetic
Word Length:	24 bits plus parity bit
Memory:	Basic 8,192 words, random access coincident current core memory with data saver in case of power interruption. Expandable in memory banks to 131,072 words
Read Cycle:	450 nanoseconds (access time)
READ/RESTORE Memory Cycle:	950 nanoseconds
Arithmetic Register:	Sign plus 23 bits magnitude, two's complement negative numbers
Execution times at 8 mHz clock rate (including Instruction Cycle)	
ADD:	1.9 μsec
MULTIPLY:	5.6 μsec
DIVISION:	7.9 μsec
Addressing:	Direct addressing for up to 131,072 words
Indirect Addressing:	Multilevel indirect addressing capability
Interrupts:	16 standard levels of priority interrupt, expandable to any amount desired
Indexing:	1 external index register which requires no additional time for operation
Command Repertoire:	70 instructions including input/output control
Precision:	Multiple length arithmetic operations in 24 bit segments i.e., 48, 72, 96, etc.
Input/Output:	1) Automatic real time I/O channel with direct memory access (1 million characters of 24 bits each, per second) 2) Multiplexed I/O under program control with priority interrupts—16 input and 16 output channels 3) Device interrupt controlled 8 bit character input channel
Power Consumption:	500 w
Operating Temperature Range:	—65 to +160°F
Size:	1.9 cubic feet
Weight:	100 pounds

instructions

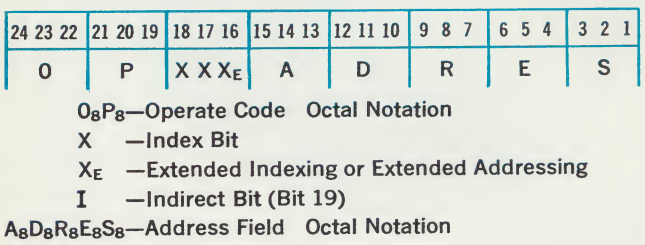
word format

Each memory word consists of 24 bits plus a parity bit. The computer automatically generates odd parity or checks for it during each read or store cycle. An indicator is present on the control panel giving a positive indication to the operator.

A computer word is 24 binary digits (bits) in length:

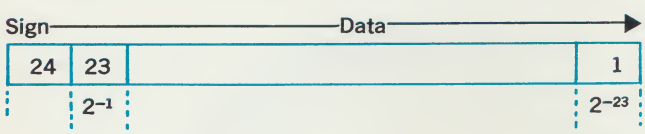
The above format numbers the bits from right to left with the least significant bit on the right, and the most significant bit on the left.

Instruction Word Format



data word format

In the memory the numbers are of the two's complement form, single precision numbers having 23 magnitude bits and a sign bit.



As indicated, the most significant bit position is the sign bit. A zero "0" in the sign bit denotes a positive number and a one "1" in the sign bit denotes a negative number. All numbers are fractional with the decimal point between bits 23 & 24. Since the value of the most significant bit is equal to 1 the largest negative number is minus 1 and the largest positive number approaches but never attains the value of plus 1.

address modification

Indexing and Indirect Addressing, used alone or in combination, provide address modification. In either case, the address portion of the instruction is read out of memory and is then modified before the instruction is executed. The original instruction is retained in memory. The resultant address used in the execution of the instruction is called the "effective address."

Indexing is performed by the use of an Index Register. Indexed instructions require no additional time for execution. If the contents of bit 17 of the Index bit is a "1", the contents of the Index Register are subtracted from the address portion of the instruction (bits 1 through 15) prior to execution. The Instruction Set contains commands for decrementing and testing the Index Register, as well as Load and Store Index Register Instructions.

INSTRUC-TION	DESCRIPTION	TIME	FUNCTION	TYPE
	ARITHMETIC INSTRUCTIONS			
ADA	ADD contents of Memory to contents of AC.	1.9 μs	C(Y) plus C(AC) → [AC] carry overflow → interrupt	Addressable
SBA	SUBtract contents of AC from contents of Memory	1.9 μs	(AC) minus C(Y) → [AC] under borrow → interrupt	Addressable
MPA	MULtiply contents of Memory to contents of AC	5.6 μs	[C(Y) times C(AC)] → [AC, MQ] $C(MQ)_{24} = C(AC)_{24}$ = product sign $C(AC)_{23-1}$ = most significant product $C(MQ)_{23-1}$ = least significant product (−1) times (−1) → Interrupt	Addressable
DVA	DIVide contents of AC and MQ by contents of memory	7.9 μs	[C(AC) divided by C(Y)] → [(MQ), (AC)] $C(MQ)_{24}$ = Quotient sign $C(MQ)_{23-1}$ = Quotient $C(MQ)_{24}$ = Remainder Sign $C(AC)_{23-1}$ = Remainder C(AC) > C(Y) → Interrupt	Addressable
EMA	Extended Multiple ADD	.95 μs	Multi precision mode for add carry overflow interrupt inhibited except on final ADD	Non-Addressable
EMS	Extended Multiple SUB	.95 μs	Multi precision mode for subtract under borrow interrupt inhibited except on final SUB	Non-Addressable
INCQ	Add one to MQ	.95 μs	C(MQ) + 1 → [MQ]	Non-Addressable
	LOGIC INSTRUCTIONS			
ANA	Contents of Memory Anded with contents of AC	1.9 μs	$\overline{C(Y)} \cdot C(AC) \rightarrow [AC]$	Addressable
ORA	Contents of Memory ORed with contents of AC	1.9 μs	C(Y) + C(AC) → [AC]	Addressable
XOA	Contents of Memory exclusively ORed with contents of AC	1.9 μs	C(Y) + C(AC) → [AC]	Addressable
	LOAD INSTRUCTIONS			
LDA	LOAD contents of Memory into AC	1.9 μs	C(Y) → [AC]	Addressable
LNA	LOAD contents of Memory into AC in two's complement form	1.9 μs	C(Y) + 1 → [AC]	Addressable
LDQ	LOAD contents of Memory into MQ	1.9 μs	C(Y) → [MQ]	Addressable
* LDX	LOAD contents of Memory into XR	1.9 μs	C(Y) → [XR]	Addressable
LDE	LOAD contents of Memory into IO Buffer A	1.9 μs	C(Y) → [IO]	Addressable
ZRA	LOAD zero into AC	.95 μs	0 → [AC]	Non-Addressable
	STORE INSTRUCTIONS			
STA	STORE contents of AC into Memory	1.9 μs	C(AC) → C(Y)	Addressable
STQ	STORE contents of MQ into Memory	1.9 μs	C(MQ) → C(Y)	Addressable
* STX	STORE contents of XR into Memory	1.9 μs	C(XR) → C(Y)	Addressable
STE	STORE contents of IO Buffer A into Memory	1.9 μs	C(IO) → C(Y)	Addressable
STZ	STORE zero into Memory	1.9 μs	0 → C(Y)	Addressable

* INDEX REGISTER is specified by index bits in instruction word.

INSTRUCTION	DESCRIPTION	TIME	FUNCTION	TYPE
TRANSFER INSTRUCTIONS				
TRS	TRANSFER to subroutine and STORE contents of PC into Memory	1.9 μs	C(PC + 1) → C(Y) Program Control → Y + 1	Addressable
TRE	TRANSFER control and enable Interrupts	.95 μs	Program Control → Y Reset Interrupt Indicators	Addressable
TRI	TRANSFER control and inhibit Interrupt	.95 μs	Program Control → Y Inhibit Interrupt Indicator Set	Addressable
TRA	TRANSFER control	.95 μs	Program Control → Y	Addressable
TRN	TRANSFER control if contents of AC is negative	.95 μs	Test $C(AC)_{24}$, sign bit $AC_{24} = 1$: Program control → Y $AC_{24} = 0$: Program control → PC + 1	Addressable
TRP	TRANSFER control if contents of AC is positive or zero	.95 μs	Test $C(AC)_{24}$, sign bit $AC_{24} = 0$: Program control → Y $AC_{24} = 1$: Program control → PC + 1	Addressable
TRZ	TRANSFER control if contents of AC is zero	.95 μs	Test zero, C(AC) = 0 Zero: Program control → Y Not zero: Program control → PC + 1	Addressable
TNZ	TRANSFER control if contents of AC is not zero	.95 μs	Test zero, C(AC) = 0 Not zero: Program control → Y Zero: Program control → PC + 1	Addressable
* TRX	TRANSFER control if contents of XR is not zero and decrement XR register	.95 μs	Test C(XR), C(XR) = 0 C(XR) ≠ 0: Program control → Y C(XR) = 1 → C(XR) C(XR) = 0: Program control → PC + 1	Addressable
INPUT/OUTPUT CONTROL				
ZRI	Clear Interrupts	.95 μs	Reset to Status indicator	Non-Addressable
SEL	SELECT input device N (Channel A) and terminate with interrupt	.95 μs	IO not busy: ID_n flag → Input device Interrupt upon receipt of word IO busy: Program control → PC + 2	Non-Addressable
SEL	SELECT output device N (Channel A) and terminate with interrupt	.95 μs	IO not busy: OD_n flag ready Next LIO, OD_n → Output device Interrupt upon transmission of word IO busy: Program control → PC + 2	Non-Addressable
SKIP INSTRUCTIONS				
SAO	SKIP to next instruction if AC OVerflow and reset interrupt logic	.95 μs	AC OV = 1: Program control → PC + 2 Reset AC OV Interrupt F/F AC OV ≠ 1: Program control → PC + 1	Non-Addressable
SNO	SKIP to next instruction if AC OVerflow not set	.95 μs	AC OV ≠ 1: Program control → PC + 2 AC OV = 1: Program control → PC + 1 Reset AC OV Interrupt F/F	Non-Addressable
SOS	SKIP to next instruction if AC and MQ signs different	.95 μs	$AC_{24} \neq MQ_{24}$: Program control → PC + 2 $AC_{24} = MQ_{24}$: Program control → PC + 1	Non-Addressable
SQP	SKIP to next instruction if MQ positive or zero	.95 μs	$MQ_{24} = 0$: Program control → PC + 2 $MQ_{24} = 1$: Program control → PC + 1	Non-Addressable
SQN	SKIP to next instruction if MQ negative	.95 μs	$MQ_{24} = 1$: Program control → PC + 2 $MQ_{24} = 0$: Program control → PC + 1	Non-Addressable
SLO	SKIP to next instruction if least significant bit is one	.95 μs	C(Y) LSB = 1: Program control → PC + 2 C(Y) LSB = 0: Program control → PC + 1	Non-Addressable
SLZ	SKIP to next instruction if least significant bit is zero	.95 μs	C(Y) LSB = 0: Program control → PC + 2 C(Y) LSB = 1: Program control → PC + 1	Non-Addressable

* INDEX REGISTER is specified by index bits in instruction word.

INSTRUC-TION	DESCRIPTION	TIME	FUNCTION	TYPE
SSH	SKIP to next instruction if sense switches high	.95 μs	**Sense Switches High** singularly or in combination } Program Control → PC + 2 Otherwise: Program control → PC + 1	Non-Addressable
SSL	SKIP to next instruction if sense switches low	.95 μs	**Sense Switches Low** singularly or in combination } Program control → PC + 2 Otherwise: Program control → PC + 1	Non-Addressable
SKP	SKIP to next instruction if paper tape parity error indicator is on	.95 μs		Non-Addressable
	MOVE INSTRUCTIONS			
MAX	MOVE contents of AC to MQ	.95 μs	C(AC) → MQ	Non-Addressable
*MAQ	MOVE contents of AC to Index Register	.95 μs	C(AC) → XR	Non-Addressable
MSA	MOVE contents of Control panel switches to AC	.95 μs	C(SW) → AC	Non-Addressable
	SHIFT INSTRUCTIONS			
LSA	SHIFT the low order bits of AC into High order bits "N" times specified by instruction format	1.125 + .125N	$C(AC)_n \rightarrow AC_{n+1}$ each shift $AC_{24} \rightarrow AC_{24}$ sign bit $0 \rightarrow AC_1$ each shift AC overflow interrupts	Non-Addressable
RSA	SHIFT the High order bits of AC into low order bits "N" times specified by instruction format	1.125 + .125N	$C(AC)_n \rightarrow AC_{n-1}$ each shift $AC_{24} \rightarrow AC_{24}$ sign bit $AC_{24} \rightarrow AC_{23}$ each shift	Non-Addressable
NLS	SHIFT the contents of the AC and MQ registers from low order bits to high order bits until most significant bit of AC is obtained	1.125 + .125N	$C(AC) \rightarrow AC_{n+1}$ each shift $AC_{24} \rightarrow AC_{24}$ sign bit $C(MQ)_n \rightarrow MQ_{n+1}$ each shift $MQ_{24} \rightarrow MQ_{24}$ sign bit $MQ_{23} \rightarrow AC_1$ each shift $0 \rightarrow MQ_1$ each shift $AC_{24} \neq AC_{23}$: stop shifting	Non-Addressable
AQ	CYCLE the contents of the AC and MQ registers from the low order bits to the high order bit "N" times specified by the instruction format	1.125 + .125N	$C(AC)_n \rightarrow AC_{n+1}$ each shift $C(MQ)_n \rightarrow MQ_{n+1}$ each shift $MQ_{24} \rightarrow AC_1$ each shift $AC_{24} \rightarrow MQ_1$ each shift	Non-Addressable
RAQ	SHIFT the contents of the AC and MQ registers from the high order bits to the low order bits "N" times specified by the instruction format	1.125 + .125N	$C(AC)_n \rightarrow AC_{n-1}$ each shift $AC_{24} \rightarrow AC_{24}$ sign bit $C(MQ)_n \rightarrow MQ_{n-1}$ each shift $AC_{24} \rightarrow MQ_{24}$ sign bit $C(AC)_1 \rightarrow MQ_{23}$ each shift $AC_{24} \rightarrow DAC_{23}$ each shift	Non-Addressable
LCA	(AC) left cycle	1.125 + .125N		
	OPERATE INSTRUCTION			
XEC	EXECUTE the instruction contained in Memory Location (Y)	.95 μs + execution of instruction	Transfer control to (Y) Return to main control on next instruction	Addressable
XNA	same as XEC if (AC) < 0			
HLT	I/O WAIT	.95 μs	HALT	Non-Addressable
NOP	No Operation	.95 μs	DO NOTHING	Non-Addressable
SMB	Transfer to alternate Memory Bank	.95 μs	Transfer control to Alternate Memory Bank Use same address field	Non-Addressable

input/output subsystem

The input/output subsystem for the R-11 gives the flexibility of tailoring I/O complexity to the particular application.

A Simplex Type A Channel will select up to 16 devices (in or out) at a minimum cost on a word by word basis.

A Simplex Type B Channel incorporates block transfer capability for up to 16 devices (in or out) and includes the capabilities of Channel A with increased speed.

The Real Time Multiplexed Type C Channel incorporates the characteristics of Channels A and B in a multiplexed priority select mode with direct access to memory for any number of devices.

Thus the input/output subsystem can be tailored to the complexity of the application. It is designed to provide the ability to perform in a real-time environment, with a wide variety of devices such as radar data buffers, PCM communications equipment, display devices, etc. Some of these devices, such as the radar interface, enter data to the processor at very high rates and are serviced on a demand basis, whereas communications and display equipment, being less severe in their transfer rates, are serviced via program control.

type A and B program controlled simplex I/O channels

This buffered input-output channel is completely under the programmer's control. Peripheral equipment such as paper tape reader and punch, keyboard, etc., and connected to the computer via this channel and operation is initiated by program control. Features such as an interrupt on completion are incorporated in order that the program may perform other tasks while waiting for the device to complete its data transmission. The entire control is accomplished with two types of instructions: load-store and device select.

input

A program can transmit data between memory and peripheral devices under the direct control of single instructions. To accomplish this, the program first must "alert" the buffer and peripheral device with an input select instruction (SEL Device No. N). The buffer is made "busy" and awaits the transfer of a character from the device. When the program is notified that the data is loaded (by means of an interrupt), data can be placed in the specified memory location by a store input/output buffer instruction without disturbing any internal registers.

output

Similar to the input operation, an output select instruction "alerts" the buffer and makes it busy. A load input/output instruction (LDE) loads the buffer with the contents of the specified memory location and signals the selected peripheral device.

Input/Output Subsystem Types

	Type A Simplex Channel	Type B Simplex Channel	Type C Real Time Multiplex Channel
Number of Devices	* 16-Input 16-Output	* 16-Input 16-Output	High Speed Multiplexing for any number of Devices
I/O Transfer Rate	7.6 μsec/word (Includes Interrupt Servicing)	950 nanosec/word Block Transfer	950 nanosec/word
Interrupt	Yes (on word completion)	Yes (on block completion)	Yes: Interrupt with priority (on block completion)
Data Mode	Single Word Transfer	Data Block Transfer	Multiplexed Data Transfer
Hardware Required:			
Device Control	One Interface Control	One Interface Control	One Interface Control with Data Buffer and Address Registers
I/O Subsystem Control	One I/O Buffer	One I/O Buffer with Address Registers	Multiplex Controller
Characteristics	Minimum Complexity Program Controlled	Increased Speed Program Controlled	Real Time High Speed, Priority Interrupts & Data Multiplexing
Advantages	Minimum Cost	High Speed Block Transfer	Designed for Real Time High Speed Data Transfer and I/O Flexibility. Multiple Memories and Processors are bussed through the Multiplexer for Multiprocessing Universal peripheral usage.

* Expansion Optional

type C. real-time multiplexed I/O data channel

This high-speed channel allows the direct transfer of data between memory and any number of external devices. The transfer, once initiated, does not require program control. The data can arrive at any time and is therefore asynchronous to the central processor. Data can be outputted or inputted at a rate exceeding one million words per second.

The multiplexed channel consists of a word size data buffer, a real time address register which provides the address of the data word to be transferred, an end address comparison register and a bus which is used to share memory with the central processor. Channel C can be selected to operate synchronously or as a high speed channel under program control.

A typical selection of channel C under program control would proceed as follows: A selection of an external device would be made via Channel C using the common select instruction. A load input/output instruction would follow if the device selected was not busy. The first load instruction would store the starting memory address (location from which data is to be taken from or put into memory) into the external real time address register. The second load instruction would load the end address into the external comparison register. The Central Processor is now free to go on executing its stored program. When the external device selected through the C channel is ready to input or output, it looks at memory to see if it is available. If at the same time the Central Processor is making a request for memory, it will lose out to channel C via priority. The only time that Channel C must wait for memory is if a memory initiate has been made previous to its request by Channel C and the memory has not completed its cycle. When Channel C is granted memory access it inputs or outputs one word from memory in one memory cycle time. This it does without using any registers internal to the central processor. This sequence continues until an address comparison is made. An address comparison interrupts the central processor and forces it to a fixed location in memory. The programmer is now free to select the same device if he wishes.

If any device tied to Channel C is operating asynchronously to the central processor then the following sequence takes place. When the external device requires an access to or from memory it interrupts the central processor and forces it to a fixed memory location. The data is now transferred to or from memory in one memory cycle. The data is again inputted or outputted without any loss of information in the active registers of the central processor.

control panel

The Control Panel is intended as an auxiliary unit to the Central Processor for the purpose of maintenance, and program modification and verification. The upper portion of the control panel contains the indicators and switches associated with the memory and the lower portion contains the indicators and control switches associated with the central processor unit.

1. *Memory Data Indicator*—Twenty-four indicators display, in binary form, the data word output from the memory.

2. *Memory Address Indicators*—Fifteen indicators display the address location of the memory data as indicated above.

3. *Memory Voltage Tests*—Visual indication of application of power is shown by the ac and dc lights. These lights have no direct control of the prime power inputs but indicate that power is applied to the power supplies of the memory and control processor unit.

However, the dc light has a built-in alternate switch from which the operator has direct control of the dc voltage. Incorporated in the dc controls is a latching relay which senses the voltage level. Should the voltage fall below a preset threshold, the relay will release all dc voltages for the protection of the memory contents.

The actual voltage levels may be measured on the meter by proper selection of the voltage test button. These switches are electrically interlocked so that only one selection can be made at a time. The switches are labeled as follows: Line (Line Voltage), R/W (Read-Write), INH (inhibit), +20(V), +6(V), and −15 (V). Only the plus six (+6) is used in the central processor.

4. *Memory Test*—The application of memory test patterns is controlled first by the memory test switch which releases or locks the test pattern switches. The operator has the option of applying the following patterns to all locations in memory: Zero's, Ones, Worst pattern, and Worst pattern complements. This set of four switches is also mechanically interlocked so that only one selection can be made at a time.

To load the test pattern selected into memory the "Load" button must be depressed. All locations in memory will be loaded.

A read/restore of each location is accomplished by depressing the unload button. Cycling the memory commences when the "clock start" button is depressed. When an error occurs the "Test error" indicator will illuminate and the location and pattern will be displayed on the "memory data" and "memory address" indicators. The "Stop Error" switch allows the operator to stop the test when the errors occur, or continues cycling overriding the error. Cycling through the memory may be accomplished manually by depressing the "Clock Step" button. Each time this switch is actuated the read/restore test is incremented to the next location in memory.

Parity errors are indicated on the "Par Error" indicator and the operate condition of the pattern generator is displayed on the "Patt Gen" indicator.

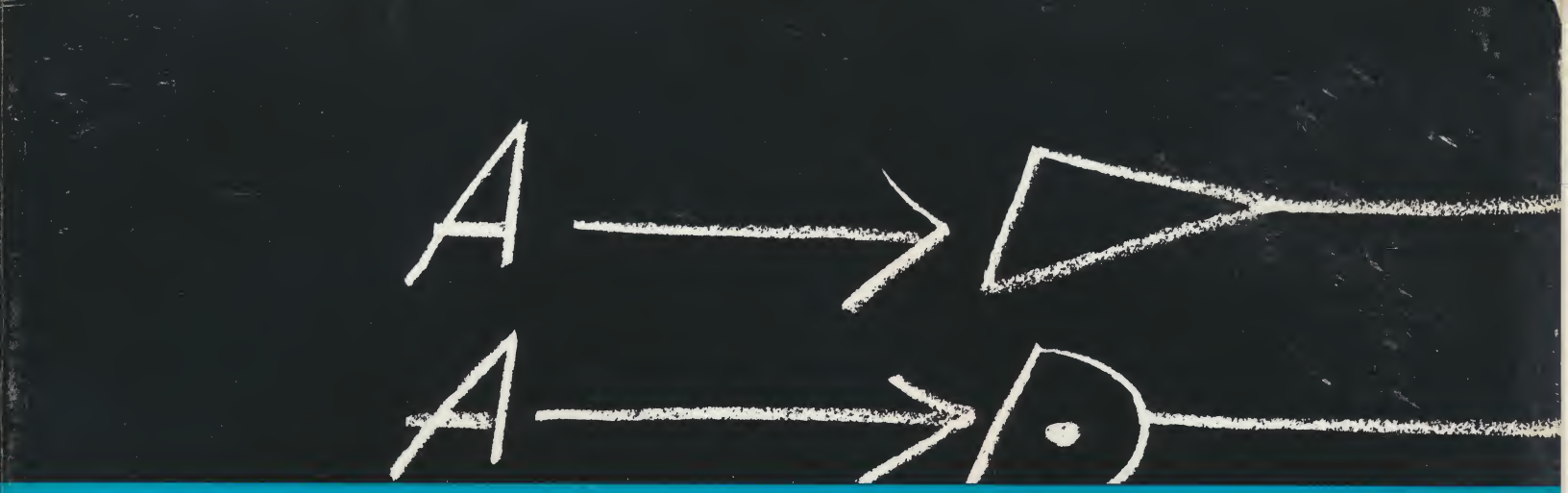
5. *Mode Control Switches AUTO, SMI, SPM*—The mode control switches are a set of three momentary switches, electronically interlocked. They are marked AUTO, placing the CPU in the automatic mode, and SIM and SPM, placing the CPU in the manual mode. Depressing any switch enables the particular switch and disables the others.

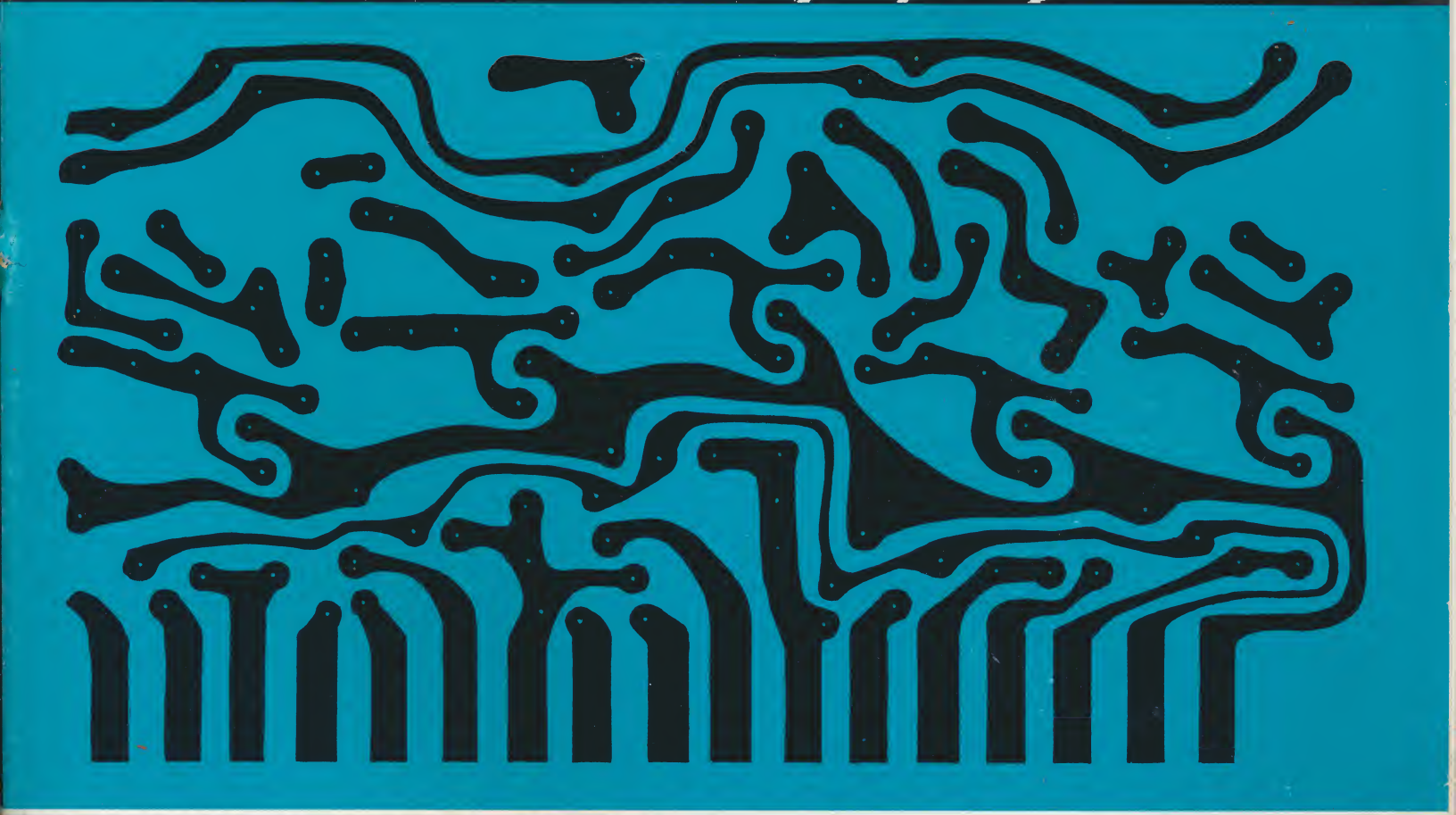
6. *Manual Load Control Switches EXE, LAC, LMQ*—The manual load control switches are a set of three momentary switches which are operative only in the manual mode, that is SIM or SPM. They are marked the EXE which loads the ME Register with the word assembled on the manual load switches, the LAC which loads the AC register from the manual load switch, and the LMQ which loads the MQ register from the manual load switch.

7. *Manual Load Switches 24 - - - 1*—The manual load switch is an array of twenty-four (24) alternate action switches from which a computer word can be assembled. When depressed, the indicator illuminates signifying a logic "1" at the selected bit location. The indicators are coded in an octal array for ease of operation. These switches operate in conjunction with the manual load control switches, EXE, LAC and LMQ.

8. *Register Display and Select Switches*—During any manual operation the operator has the option to observe the contents of below listed registers on the Register Display indicators by depressing the corresponding Register Display Select switch which illuminates.

9. *Start, Stop Switch*—Either the start or stop switch will be illuminated depending on the run status of the central processor unit.





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READ/RESTORE Memory Cycle:	950 nanoseconds
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MULTIPLY:	5.6 μsec
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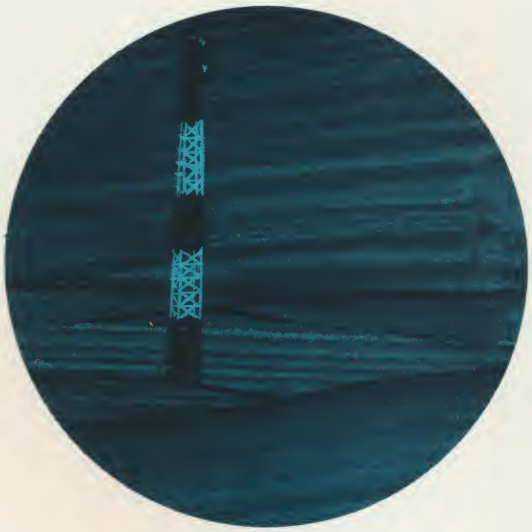
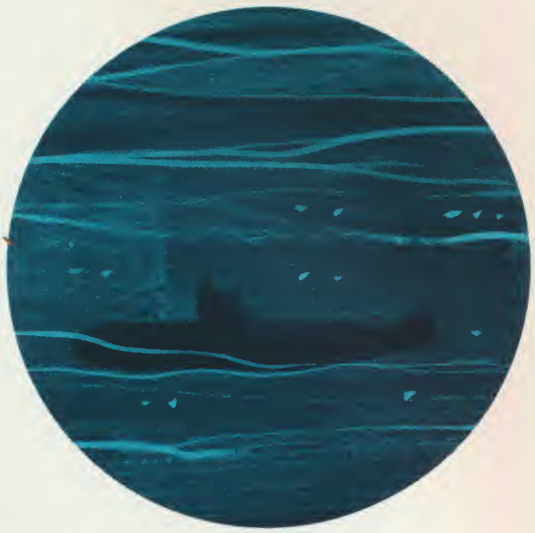
Weight:	100 pounds

applications

The size and weight of the R-11 makes it ideally suited to use over a broad range of operational environments. Now, in a previously unattainable package, the means exists to deploy to any point on earth the complete self-contained capability of tactical command and control data reduction systems, fire control, communication switching, and missile checkout.

Application of the R-11 in an airborne, spaceborne, or undersea environment makes possible the centralization of vehicle and payload data processing functions. Small size combined with high reliability lends itself to the requirements of system weight and volume limitations. Navigation, attitude control, inflight performance monitoring, sensor data manipulation, and communications are all within the range of control by the R-11. This computer-display-control complex, properly coupled with the human interface, provides for completely integrated data management and decision-making.





instructions

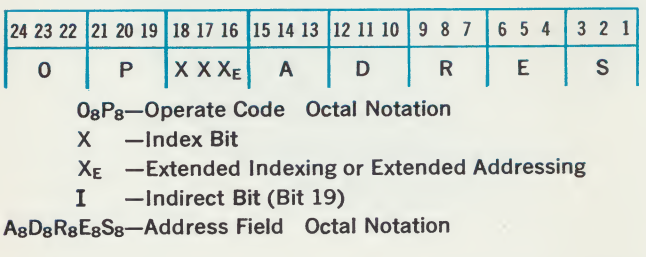
word format

Each memory word consists of 24 bits plus a parity bit. The computer automatically generates odd parity or checks for it during each read or store cycle. An indicator is present on the control panel giving a positive indication to the operator.

A computer word is 24 binary digits (bits) in length:

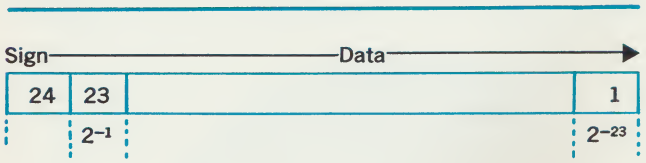
The above format numbers the bits from right to left with the least significant bit on the right, and the most significant bit on the left.

Instruction Word Format



data word format

In the memory the numbers are of the two's complement form, single precision numbers having 23 magnitude bits and a sign bit.



As indicated, the most significant bit position is the sign bit. A zero "0" in the sign bit denotes a positive number and a one "1" in the sign bit denotes a negative number. All numbers are fractional with the decimal point between bits 23 & 24. Since the value of the most significant bit is equal to 1 the largest negative number is minus 1 and the largest positive number approaches but never attains the value of plus 1.

address modification

Indexing and Indirect Addressing, used alone or in combination, provide address modification. In either case, the address portion of the instruction is read out of memory and is then modified before the instruction is executed. The original instruction is retained in memory. The resultant address used in the execution of the instruction is called the "effective address."

Indexing is performed by the use of an Index Register. Indexed instructions require no additional time for execution. If the contents of bit 17 of the Index bit is a "1", the contents of the Index Register are subtracted from the address portion of the instruction (bits 1 through 15) prior to execution. The Instruction Set contains commands for decrementing and testing the Index Register, as well as Load and Store Index Register Instructions.

INSTRUC-TION	DESCRIPTION	TIME	FUNCTION	TYPE
	ARITHMETIC INSTRUCTIONS			
ADA	ADD contents of Memory to contents of AC.	1.9 μs	C(Y) plus C(AC) → [AC] carry overflow → interrupt	Addressable
SBA	SUBtract contents of AC from contents of Memory	1.9 μs	(AC) minus C(Y) → [AC] under borrow → interrupt	Addressable
MPA	MULtiply contents of Memory to contents of AC	5.6 μs	[C(Y) times C(AC)] → [AC, MQ] $C(MQ)_{24} = C(AC)_{24}$ = product sign $C(AC)_{23-1}$ = most significant product $C(MQ)_{23-1}$ = least significant product (−1) times (−1) → Interrupt	Addressable
DVA	DIVide contents of AC and MQ by contents of memory	7.9 μs	[C(AC) divided by C(Y)] → [(MQ), (AC)] $C(MQ)_{24}$ = Quotient sign $C(MQ)_{23-1}$ = Quotient $C(MQ)_{24}$ = Remainder Sign $C(AC)_{23-1}$ = Remainder C(AC) > C(Y) → Interrupt	Addressable
EMA	Extended Multiple ADD	.95 μs	Multi precision mode for add carry overflow interrupt inhibited except on final ADD	Non-Addressable
EMS	Extended Multiple SUB	.95 μs	Multi precision mode for subtract under borrow interrupt inhibited except on final SUB	Non-Addressable
INCQ	Add one to MQ	.95 μs	C(MQ) + 1 → [MQ]	Non-Addressable
	LOGIC INSTRUCTIONS			
ANA	Contents of Memory Anded with contents of AC	1.9 μs	$\overline{C(Y)}$ • C(AC) → [AC]	Addressable
ORA	Contents of Memory ORed with contents of AC	1.9 μs	C(Y) + C(AC) → [AC]	Addressable
XOA	Contents of Memory exclusively ORed with contents of AC	1.9 μs	C(Y) + C(AC) → [AC]	Addressable
	LOAD INSTRUCTIONS			
LDA	LOAD contents of Memory into AC	1.9 μs	C(Y) → [AC]	Addressable
LNA	LOAD contents of Memory into AC in two's complement form	1.9 μs	C(Y) + 1 → [AC]	Addressable
LDQ	LOAD contents of Memory into MQ	1.9 μs	C(Y) → [MQ]	Addressable
* LDX	LOAD contents of Memory into XR	1.9 μs	C(Y) → [XR]	Addressable
LDE	LOAD contents of Memory into IO Buffer A	1.9 μs	C(Y) → [IO]	Addressable
ZRA	LOAD zero into AC	.95 μs	0 → [AC]	Non-Addressable
	STORE INSTRUCTIONS			
STA	STORE contents of AC into Memory	1.9 μs	C(AC) → C(Y)	Addressable
STQ	STORE contents of MQ into Memory	1.9 μs	C(MQ) → C(Y)	Addressable
* STX	STORE contents of XR into Memory	1.9 μs	C(XR) → C(Y)	Addressable
STE	STORE contents of IO Buffer A into Memory	1.9 μs	C(IO) → C(Y)	Addressable
STZ	STORE zero into Memory	1.9 μs	0 → C(Y)	Addressable

* INDEX REGISTER is specified by index bits in instruction word.

INSTRUCTION	DESCRIPTION	TIME	FUNCTION	TYPE
TRANSFER INSTRUCTIONS				
TRS	TRANSFER to subroutine and STORE contents of PC into Memory	1.9 μs	C(PC + 1) → C(Y) Program Control → Y + 1	Addressable
TRE	TRANSFER control and enable Interrupts	.95 μs	Program Control → Y Reset Interrupt Indicators	Addressable
TRI	TRANSFER control and inhibit Interrupt	.95 μs	Program Control → Y Inhibit Interrupt Indicator Set	Addressable
TRA	TRANSFER control	.95 μs	Program Control → Y	Addressable
TRN	TRANSFER control if contents of AC is negative	.95 μs	Test $C(AC)_{24}$, sign bit $AC_{24} = 1$: Program control → Y $AC_{24} = 0$: Program control → PC + 1	Addressable
TRP	TRANSFER control if contents of AC is positive or zero	.95 μs	Test $C(AC)_{24}$, sign bit $AC_{24} = 0$: Program control → Y $AC_{24} = 1$: Program control → PC + 1	Addressable
TRZ	TRANSFER control if contents of AC is zero	.95 μs	Test zero, C(AC) = 0 Zero: Program control → Y Not zero: Program control → PC + 1	Addressable
TNZ	TRANSFER control if contents of AC is not zero	.95 μs	Test zero, C(AC) = 0 Not zero: Program control → Y Zero: Program control → PC + 1	Addressable
* TRX	TRANSFER control if contents of XR is not zero and decrement XR register	.95 μs	Test C(XR), C(XR) = 0 C(XR) ≠ 0: Program control → Y C(XR) = 1 → C(XR) C(XR) = 0: Program control → PC + 1	Addressable
INPUT/OUTPUT CONTROL				
ZRI	Clear Interrupts	.95 μs	Reset to Status indicator	Non-Addressable
SEL	SELECT input device N (Channel A) and terminate with interrupt	.95 μs	IO not busy: ID_n flag → Input device Interrupt upon receipt of word IO busy: Program control → PC + 2	Non-Addressable
SEL	SELECT output device N (Channel A) and terminate with interrupt	.95 μs	IO not busy: OD_n flag ready Next LIO_t OD_n → Output device Interrupt upon transmission of word IO busy: Program control → PC + 2	Non-Addressable
SKIP INSTRUCTIONS				
SAO	SKIP to next instruction if AC OVerflow and reset interrupt logic	.95 μs	AC OV = 1: Program control → PC + 2 Reset AC OV Interrupt F/F AC OV ≠ 1: Program control → PC + 1	Non-Addressable
SNO	SKIP to next instruction if AC OVerflow not set	.95 μs	AC OV ≠ 1: Program control → PC + 2 AC OV = 1: Program control → PC + 1 Reset AC OV Interrupt F/F	Non-Addressable
SOS	SKIP to next instruction if AC and MQ signs different	.95 μs	$AC_{24} \neq MQ_{24}$: Program control → PC + 2 $AC_{24} = MQ_{24}$: Program control → PC + 1	Non-Addressable
SQP	SKIP to next instruction if MQ positive or zero	.95 μs	$MQ_{24} = 0$: Program control → PC + 2 $MQ_{24} = 1$: Program control → PC + 1	Non-Addressable
SQN	SKIP to next instruction if MQ negative	.95 μs	$MQ_{24} = 1$: Program control → PC + 2 $MQ_{24} = 0$: Program control → PC + 1	Non-Addressable
SLO	SKIP to next instruction if least significant bit is one	.95 μs	C(Y) LSB = 1: Program control → PC + 2 C(Y) LSB = 0: Program control → PC + 1	Non-Addressable
SLZ	SKIP to next instruction if least significant bit is zero	.95 μs	C(Y) LSB = 0: Program control → PC + 2 C(Y) LSB = 1: Program control → PC + 1	Non-Addressable

* INDEX REGISTER is specified by index bits in instruction word.

INSTRUCTION	DESCRIPTION	TIME	FUNCTION	TYPE
SSH	SKIP to next instruction if sense switches high	.95 μs	**Sense Switches High** singularly or in combination } Program Control → PC + 2 Otherwise: Program control → PC + 1	Non-Addressable
SSL	SKIP to next instruction if sense switches low	.95 μs	**Sense Switches Low** singularly or in combination } Program control → PC + 2 Otherwise: Program control → PC + 1	Non-Addressable
SKP	SKIP to next instruction if paper tape parity error indicator is on	.95 μs		Non-Addressable
	MOVE INSTRUCTIONS			
MAX	MOVE contents of AC to MQ	.95 μs	C(AC) → MQ	Non-Addressable
*MAQ	MOVE contents of AC to Index Register	.95 μs	C(AC) → XR	Non-Addressable
MSA	MOVE contents of Control panel switches to AC	.95 μs	C(SW) → AC	Non-Addressable
	SHIFT INSTRUCTIONS			
LSA	SHIFT the low order bits of AC into High order bits "N" times specified by instruction format	1.125 + .125N	$C(AC)_n \rightarrow AC_{n+1}$ each shift $AC_{24} \rightarrow AC_{24}$ sign bit $0 \rightarrow AC_1$ each shift AC overflow interrupts	Non-Addressable
RSA	SHIFT the High order bits of AC into low order bits "N" times specified by instruction format	1.125 + .125N	$C(AC)_n \rightarrow AC_{n-1}$ each shift $AC_{24} \rightarrow AC_{24}$ sign bit $AC_{24} \rightarrow AC_{23}$ each shift	Non-Addressable
NLS	SHIFT the contents of the AC and MQ registers from low order bits to high order bits until most significant bit of AC is obtained	1.125 + .125N	$C(AC) \rightarrow AC_{n+1}$ each shift $AC_{24} \rightarrow AC_{24}$ sign bit $C(MQ)_n \rightarrow MQ_{n+1}$ each shift $MQ_{24} \rightarrow MQ_{24}$ sign bit $MQ_{23} \rightarrow AC_1$ each shift $0 \rightarrow MQ_1$ each shift $AC_{24} \neq AC_{23}$: stop shifting	Non-Addressable
AQ	CYCLE the contents of the AC and MQ registers from the low order bits to the high order bit "N" times specified by the instruction format	1.125 + .125N	$C(AC)_n \rightarrow AC_{n+1}$ each shift $C(MQ)_n \rightarrow MQ_{n+1}$ each shift $MQ_{24} \rightarrow AC_1$ each shift $AC_{24} \rightarrow MQ_1$ each shift	Non-Addressable
RAQ	SHIFT the contents of the AC and MQ registers from the high order bits to the low order bits "N" times specified by the instruction format	1.125 + .125N	$C(AC)_n \rightarrow AC_{n-1}$ each shift $AC_{24} \rightarrow AC_{24}$ sign bit $C(MQ)_n \rightarrow MQ_{n-1}$ each shift $AC_{24} \rightarrow MQ_{24}$ sign bit $C(AC)_1 \rightarrow MQ_{23}$ each shift $AC_{24} \rightarrow DAC_{23}$ each shift	Non-Addressable
LCA	(AC) left cycle	1.125 + .125N		
	OPERATE INSTRUCTION			
XEC	EXECUTE the instruction contained in Memory Location (Y)	.95 μs + execution of instruction	Transfer control to (Y) Return to main control on next instruction	Addressable
XNA	same as XEC if (AC) < 0			
HLT	I/O WAIT	.95 μs	HALT	Non-Addressable
NOP	No Operation	.95 μs	DO NOTHING	Non-Addressable
SMB	Transfer to alternate Memory Bank	.95 μs	Transfer control to Alternate Memory Bank Use same address field	Non-Addressable

input/output subsystem

The input/output subsystem for the R-11 gives the flexibility of tailoring I/O complexity to the particular application.

A Simplex Type A Channel will select up to 16 devices (in or out) at a minimum cost on a word by word basis.

A Simplex Type B Channel incorporates block transfer capability for up to 16 devices (in or out) and includes the capabilities of Channel A with increased speed.

The Real Time Multiplexed Type C Channel incorporates the characteristics of Channels A and B in a multiplexed priority select mode with direct access to memory for any number of devices.

Thus the input/output subsystem can be tailored to the complexity of the application. It is designed to provide the ability to perform in a real-time environment, with a wide variety of devices such as radar data buffers, PCM communications equipment, display devices, etc. Some of these devices, such as the radar interface, enter data to the processor at very high rates and are serviced on a demand basis, whereas communications and display equipment, being less severe in their transfer rates, are serviced via program control.

type A and B program controlled simplex I/O channels

This buffered input-output channel is completely under the programmer's control. Peripheral equipment such as paper tape reader and punch, keyboard, etc., and connected to the computer via this channel and operation is initiated by program control. Features such as an interrupt on completion are incorporated in order that the program may perform other tasks while waiting for the device to complete its data transmission. The entire control is accomplished with two types of instructions: load-store and device select.

input

A program can transmit data between memory and peripheral devices under the direct control of single instructions. To accomplish this, the program first must "alert" the buffer and peripheral device with an input select instruction (SEL Device No. N). The buffer is made "busy" and awaits the transfer of a character from the device. When the program is notified that the data is loaded (by means of an interrupt), data can be placed in the specified memory location by a store input/output buffer instruction without disturbing any internal registers.

output

Similar to the input operation, an output select instruction "alerts" the buffer and makes it busy. A load input/output instruction (LDE) loads the buffer with the contents of the specified memory location and signals the selected peripheral device.

Input/Output Subsystem Types

	Type A Simplex Channel	Type B Simplex Channel	Type C Real Time Multiplex Channel
Number of Devices	* 16-Input 16-Output	* 16-Input 16-Output	High Speed Multiplexing for any number of Devices
I/O Transfer Rate	7.6 μsec/word (Includes Interrupt Servicing)	950 nanosec/word Block Transfer	950 nanosec/word
Interrupt	Yes (on word completion)	Yes (on block completion)	Yes: Interrupt with priority (on block completion)
Data Mode	Single Word Transfer	Data Block Transfer	Multiplexed Data Transfer
Hardware Required:			
Device Control	One Interface Control	One Interface Control	One Interface Control with Data Buffer and Address Registers
I/O Subsystem Control	One I/O Buffer	One I/O Buffer with Address Registers	Multiplex Controller
Characteristics	Minimum Complexity Program Controlled	Increased Speed Program Controlled	Real Time High Speed, Priority Interrupts & Data Multiplexing
Advantages	Minimum Cost	High Speed Block Transfer	Designed for Real Time High Speed Data Transfer and I/O Flexibility. Multiple Memories and Processors are bussed through the Multiplexer for Multiprocessing Universal peripheral usage.

* Expansion Optional

type C. real-time multiplexed I/O data channel

This high-speed channel allows the direct transfer of data between memory and any number of external devices. The transfer, once initiated, does not require program control. The data can arrive at any time and is therefore asynchronous to the central processor. Data can be outputted or inputted at a rate exceeding one million words per second.

The multiplexed channel consists of a word size data buffer, a real time address register which provides the address of the data word to be transferred, an end address comparison register and a bus which is used to share memory with the central processor. Channel C can be selected to operate synchronously or as a high speed channel under program control.

A typical selection of channel C under program control would proceed as follows: A selection of an external device would be made via Channel C using the common select instruction. A load input/output instruction would follow if the device selected was not busy. The first load instruction would store the starting memory address (location from which data is to be taken from or put into memory) into the external real time address register. The second load instruction would load the end address into the external comparison register. The Central Processor is now free to go on executing its stored program. When the external device selected through the C channel is ready to input or output, it looks at memory to see if it is available. If at the same time the Central Processor is making a request for memory, it will lose out to channel C via priority. The only time that Channel C must wait for memory is if a memory initiate has been made previous to its request by Channel C and the memory has not completed its cycle. When Channel C is granted memory access it inputs or outputs one word from memory in one memory cycle time. This it does without using any registers internal to the central processor. This sequence continues until an address comparison is made. An address comparison interrupts the central processor and forces it to a fixed location in memory. The programmer is now free to select the same device if he wishes.

If any device tied to Channel C is operating asynchronously to the central processor then the following sequence takes place. When the external device requires an access to or from memory it interrupts the central processor and forces it to a fixed memory location. The data is now transferred to or from memory in one memory cycle. The data is again inputted or outputted without any loss of information in the active registers of the central processor.

control panel

The Control Panel is intended as an auxiliary unit to the Central Processor for the purpose of maintenance, and program modification and verification. The upper portion of the control panel contains the indicators and switches associated with the memory and the lower portion contains the indicators and control switches associated with the central processor unit.

1. *Memory Data Indicator*—Twenty-four indicators display, in binary form, the data word output from the memory.

2. *Memory Address Indicators*—Fifteen indicators display the address location of the memory data as indicated above.

3. *Memory Voltage Tests*—Visual indication of application of power is shown by the ac and dc lights. These lights have no direct control of the prime power inputs but indicate that power is applied to the power supplies of the memory and control processor unit.

However, the dc light has a built-in alternate switch from which the operator has direct control of the dc voltage. Incorporated in the dc controls is a latching relay which senses the voltage level. Should the voltage fall below a preset threshold, the relay will release all dc voltages for the protection of the memory contents.

The actual voltage levels may be measured on the meter by proper selection of the voltage test button. These switches are electrically interlocked so that only one selection can be made at a time. The switches are labeled as follows: Line (Line Voltage), R/W (Read-Write), INH (inhibit), +20(V), +6(V), and −15 (V). Only the plus six (+6) is used in the central processor.

4. *Memory Test*—The application of memory test patterns is controlled first by the memory test switch which releases or locks the test pattern switches. The operator has the option of applying the following patterns to all locations in memory: Zero's, Ones, Worst pattern, and Worst pattern complements. This set of four switches is also mechanically interlocked so that only one selection can be made at a time.

To load the test pattern selected into memory the "Load" button must be depressed. All locations in memory will be loaded.

A read/restore of each location is accomplished by depressing the unload button. Cycling the memory commences when the "clock start" button is depressed. When an error occurs the "Test error" indicator will illuminate and the location and pattern will be displayed on the "memory data" and "memory address" indicators. The "Stop Error" switch allows the operator to stop the test when the errors occur, or continues cycling overriding the error. Cycling through the memory may be accomplished manually by depressing the "Clock Step" button. Each time this switch is actuated the read/restore test is incremented to the next location in memory.

Parity errors are indicated on the "Par Error" indicator and the operate condition of the pattern generator is displayed on the "Patt Gen" indicator.

5. *Mode Control Switches AUTO, SMI, SPM*—The mode control switches are a set of three momentary switches, electronically interlocked. They are marked AUTO, placing the CPU in the automatic mode, and SIM and SPM, placing the CPU in the manual mode. Depressing any switch enables the particular switch and disables the others.

6. *Manual Load Control Switches EXE, LAC, LMQ*—The manual load control switches are a set of three momentary switches which are operative only in the manual mode, that is SIM or SPM. They are marked the EXE which loads the ME Register with the word assembled on the manual load switches, the LAC which loads the AC register from the manual load switch, and the LMQ which loads the MQ register from the manual load switch.

7. *Manual Load Switches 24 - - - 1*—The manual load switch is an array of twenty-four (24) alternate action switches from which a computer word can be assembled. When depressed, the indicator illuminates signifying a logic "1" at the selected bit location. The indicators are coded in an octal array for ease of operation. These switches operate in conjunction with the manual load control switches, EXE, LAC and LMQ.

8. *Register Display and Select Switches*—During any manual operation the operator has the option to observe the contents of below listed registers on the Register Display indicators by depressing the corresponding Register Display Select switch which illuminates.

9. *Start, Stop Switch*—Either the start or stop switch will be illuminated depending on the run status of the central processor unit.

Indicators	Signal
1-6	MC, through MC6
7-10	ION, through ION4
11	IOR
12	TI
13	IOBF
14	IOB
15	Load
16	Not Used
17	Memory Read
18	Not Used
19	Indirect Mode
20	Instruction Cycle
21	Execute Cycle
22	Trap Cycle
23	Real-time Cycle
24	AC Overflow

10. *Load LT*—The load button is a momentary switch used for control of the paper tape unit. Actuating it automatically transfers the starting address to an input address register and enables the forward speed of the paper tape unit. Henceforth, the characters on the paper tape will be stored into memory uninhibited.

11. *Pulser and Timing Indicators*—The Pulser is a momentary switch that is operative only in the single pulse mode, SPM. Actuating the PLS step, the timing counter to the next time slot. The current time slot is displayed on the timing indicators.

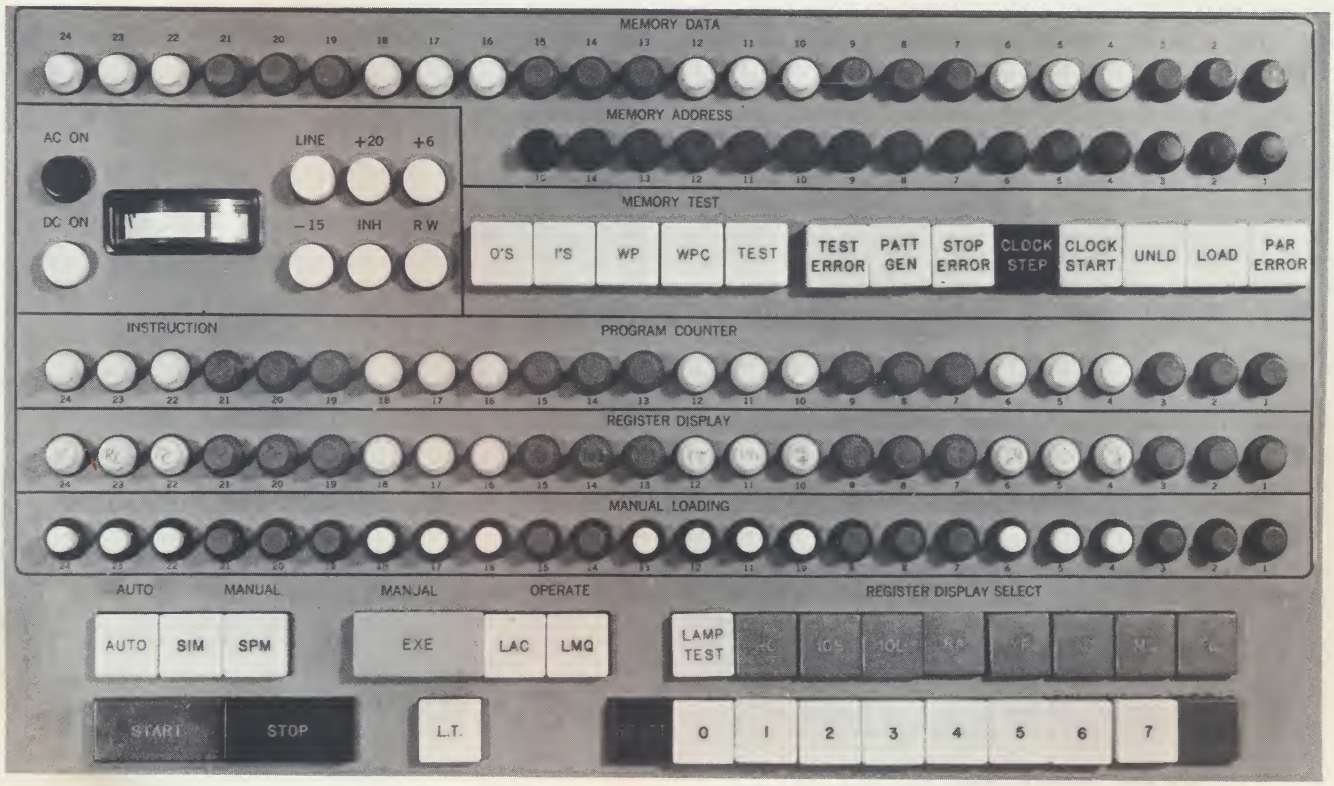
12. *Instruction and Program Counter Indicator*—Displayed continuously are the contents of the Instruction Register and the Program Counter.

13. *Reset*—All of the registers of the CPU are initialized by actuating the RESET button. The initial state of the MA register is 0 0 0 1_8 while all others are zero.

14. *Lamp Test*—The Lamp Test switch, when actuated, illuminates all indicators of the Control Panel.

Auxiliary Control Panel

The Auxiliary Control Panel contains minimum controls for operation of the computer at local or remote stations. The controls are START, STOP, and RESET. The computer operates only in the automatic mode.



machine structure

The circuitry and packaging techniques employed in the R-11 computer ensure high reliability and availability in the operational environment. One of the first considerations in building high speed digital logic is the signal wire length and therefore stray capacitance which affects overall system speed. A practical method of packaging these circuits was evolved which is intended to provide a low module cost, ease of maintenance, and maintain high speed logic on the same module.

The module size allows for a maximum number of 30 flat packs in a module, or 15 per printed circuit board, since two boards are incorporated in a frame to form a module. Each printed circuit board is etched on both sides to give the maximum number of interconnections on the card. Since speed is all important, this reduces the number of external connections necessary.

The aluminum frame is physically connected to the system ground to provide some degree of shielding from RFI. Connector pins are molded in a single phenolic block. This configuration results in less than one picofarad pin to pin capacitance.

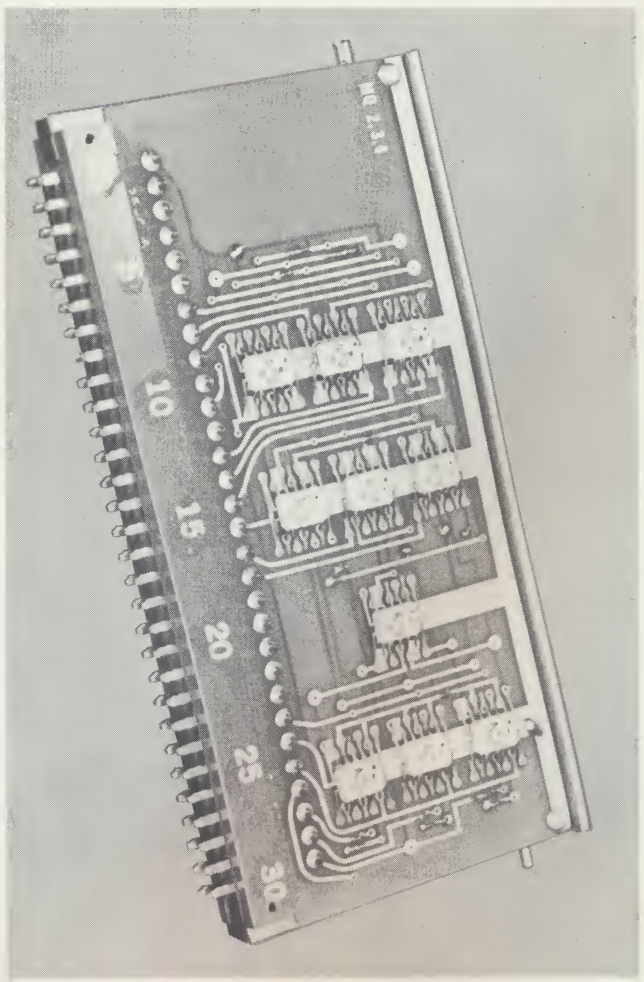
The flat packs are gap-soldered into the printed circuit board. Gap soldering was used in order to provide a low temperature connection to the integrated circuit. This method has the definite advantage of allowing the removal of any faulty flat pack. Welding the leads does not allow this flexibility.

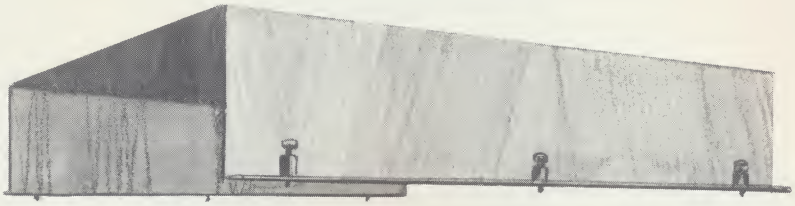
A total of 79 circuit modules are employed in the central processor and the input-output control. There are only 19 module types. Each type of module is keyed such that it is not possible to place a module in a wrong slot. In addition to this, the power is supplied on the same pins for every card in order that no damage can be done by forcing a module into the wrong slot.

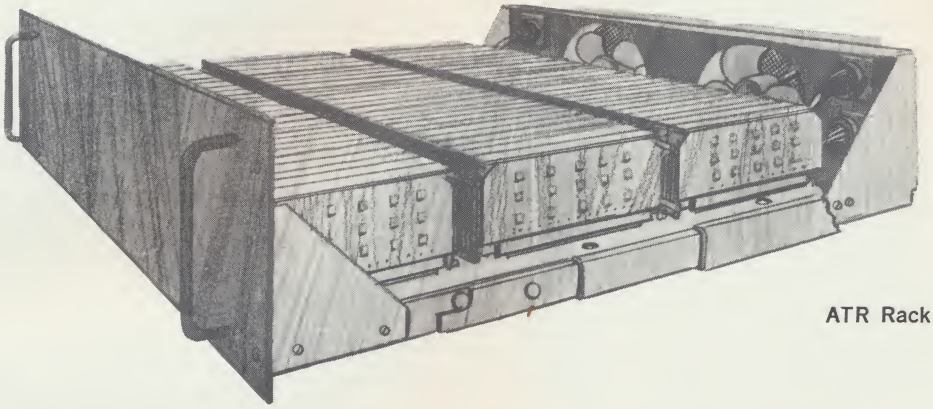
To obtain a minimum size the computer was built in a rugged, functional housing. Not only were size and weight prime considerations, but also the ease of maintenance. the housing was divided into the 1) base plate and plenum, 2) main frame, 3) memory assembly, and 4) module parent board to provide the necessary features.

The machine can be packaged to meet the customer's needs. Two basic final packages are illustrated: a control desk type arrangement or a standard ATR drawer setup.

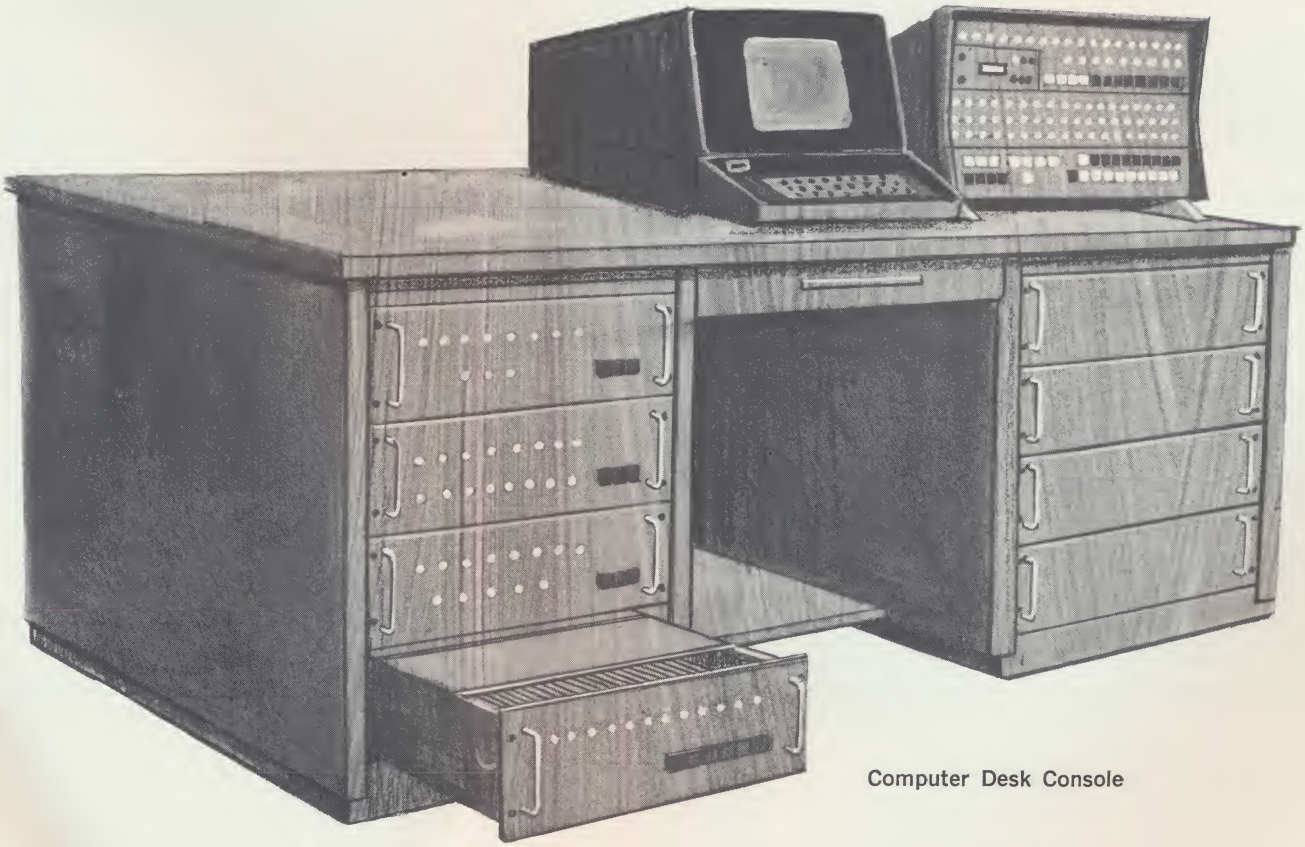
Circuit Modules







ATR Rack Drawer



Computer Desk Console

software

programming

RAP1 is a symbolic programming system for the R-11 family of digital computers. The language of RAP1 consists of octal, symbolic or mixed representations of both instruction codes and memory addresses and a complete set of both assembly action operators and pseudo operations to control the assembly of a symbolic program into a direct machine language object program.

The RAP1 programming system functions with any basic R-11 computer having punched paper tape input and digital information display system (DIDS) output for symbol lists and error messages. The number of different symbols, other than the standard set of machine language mnemonics, that may be specified in a single program is dependent upon the memory size of the R-11 computer. With a standard 8192 word memory over a thousand such symbols may be specified, even if the entire READ (RED1, RAP1, ROD1) utility package is in memory.

Editor

The R-11 alphanumeric text editor, RED1, gives the ability to read, correct, punch, augment or type out a symbolic tape text.

Program Diagnostic Routines

The R-11 on-line debugging program, ROD1, is a routine to facilitate loading, dumping memory, listing, duplicating and tracing of programs to be checked out.

Functions

The mathematical function routines for the R-11 include both single and double precision versions of: sine, cosine, arctangent, square root, natural logarithm and exponential.

peripheral equipment

Equipment available for inclusion with the R-11 includes a digital information display system, digital tape memory system, tape reader, and standard teletypewriter.

peripheral equipment characteristics

Magnetic Tape Unit—Ampex TM-11 (96 kHz).
Paper Tape Reader—Photounits 500 (500 characters/sec.)
Paper Tape Punch—Tally P-150 (150 characters/sec).
Teletypewriter—Teletype Model 33.

digital information display system

The DIDS-400 Display System is one of a series of commercial cathode ray tube (CRT) displays developed by Raytheon to meet the needs of industry and government for quick response, on-line communication with digital computers. This system meets the requirements for airline reservation systems, library data retrieval, customer files, inventory control, and numerous other applications.

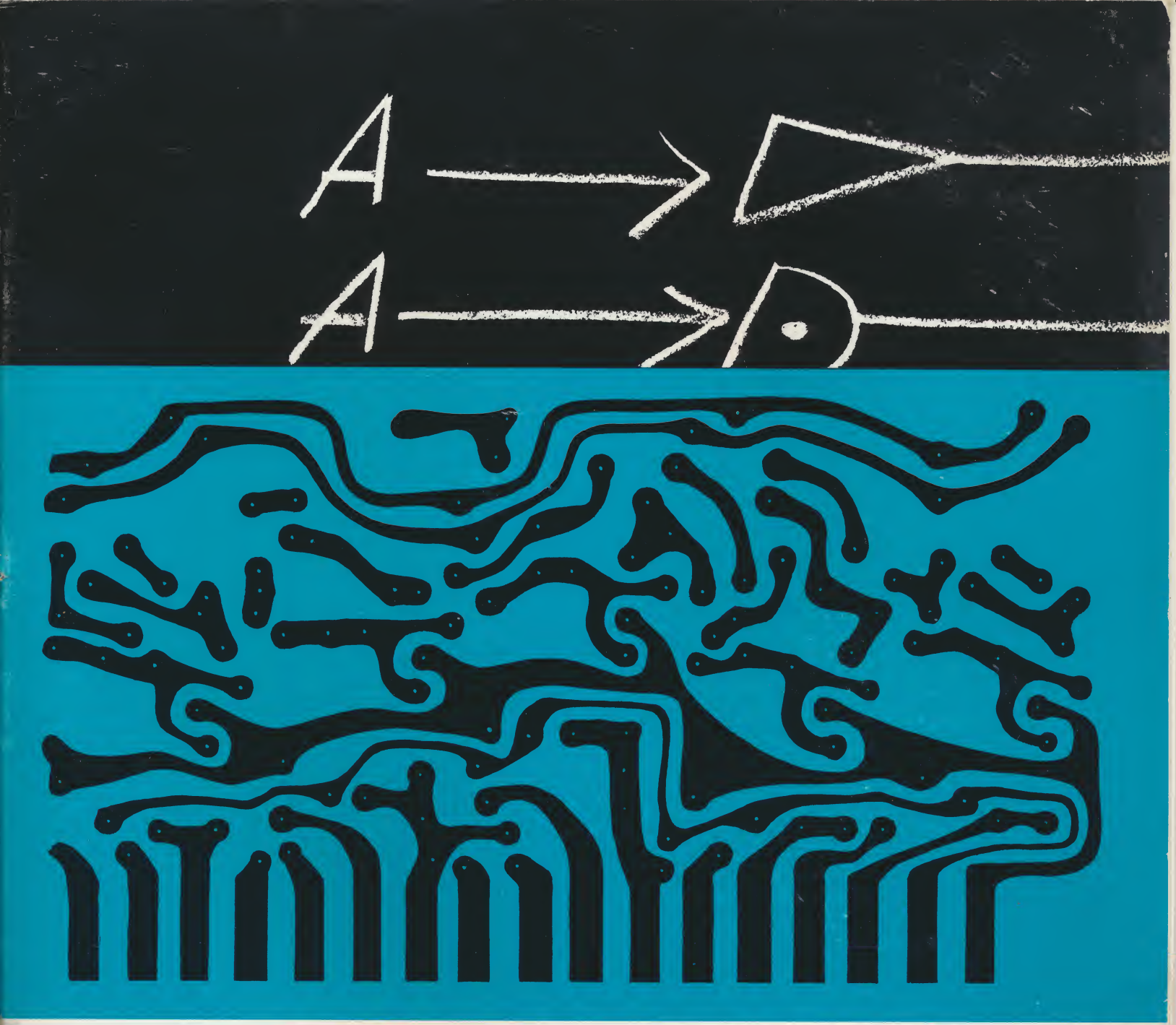
Basically the DIDS-400 system consists of a series of cathode ray tube data display consoles, matching control units, and accessories. The display consoles are available with character formats handling up to 520 or 1040 flicker-free characters. Other size display formats are available on order.

DIDS-400 operational characteristics

Display Character Capacity 520 or 1040 characters in standard model.
Display Format 520 characters—13 lines, 40 characters/line 1040 characters—26 lines, 40 characters/line Number of lines and number of characters per line can be adjustea to meet customer requirements.
Character Repertoire 62 characters: 26 alphabetic characters, 10 digits, 26 symbols.
Character Codes BCD, ASCII or other.
Typical Character Size Height: 0.17 inch, width 0.14 inch. Adjustable to meet customer format.
Viewing Surface—Standard Model 6½ by 8½ inches
Display Unit Size Height: 14½ inches, width: 16½ inches, depth: 20 inches Keyboard adds 6½ inches to depth.
Power Requirement 115 vac, 50 or 60 Hz, 200 W.

DIDS-400

MSD 46 (2.5K)11 – 66 Printed in U.S.A.



R-11

Microelectronic Computer

RAYTHEON COMPANY • MISSILE SYSTEMS DIVISION

Library Technology Reports / Data Processing

June 1, 1964

THE MEDLARS PROJECT

By Joseph Becker

This is the first of an informal series of articles which the Library Technology Project is making available to the Bulletin. *Mr. Becker is an engineer and a librarian. He has had wide experience with governmental and commercial agencies as a consultant on data processing equipment, including service to ALA on the Library 21 and Library/USA World's Fair exhibits in Seattle and New York. His* Information Storage and Retrieval, *written with R. M. Hayes, was published late in 1963.*

Future articles will describe one or more significant computer projects in libraries, and may include a round-up of new developments. Since the Library Technology Project maintains a clearinghouse of information in this area, librarians are invited to send news items on their proposed plans or programs for use of computers and other data processing equipment to David Hoffman of the LTP staff at ALA headquarters. Another ALA unit interested in developments in this area is the Interdivisional Committee on Documentation of which Maurice F. Tauber of the Columbia University library school is chairman.

There are two main classes of computers—analog and digital. *Webster's Third New International Dictionary* defines the analog computer as a "type of calculating machine that operates with numbers represented by directly measurable quantities (as voltages, resistances, or rotations)," and the digital computer as "a computer that operates with numbers expressed directly as digits in a decimal, binary, or other system."

It is extremely unlikely that the analog computer will ever find a home in the library. Analog computers are generally used to control industrial processes, missiles in flight, etc. In oil refineries, for example, they supply the necessary automation for the simultaneous adjustment of thousands of valves. These valves regulate the kind and quantity of raw material which must flow through the jungle gym of pipes in order ultimately to produce gasoline of uniform quality.

To fix the two types of computers clearly in mind, one can think of the slide rule as representing the analog computer and the Chinese abacus as representing the digital computer. The slide rule provides a graduated scale; the abacus is operated bead by bead. Since numbers may be coded to represent the letters of the alphabet in the digital computer, it holds the major promise for handling verbal data and therefore is apt to have the greater impact on library methodology.

Logic and programming

Although the inventors of the digital computer initially designed their machines to contend with burdensome forms of arithmetical data, they also made the machines capable of performing logical operations. This is the really unique feature of the digital computer because its "logic" gives it the ability to select one of a number of alternative procedures according to the outcome of some previous computation. It is capable of making comparisons between two numbers to decide if a "greater than," "less than," or "equal to" condition exists. Thus, by substituting coded numbers for letters of the alphabet, the digital computer can be programmed to make decisions based on comparisons of nonnumerical data as well. This ability to make comparisons gives the computer its greatest power in the field of information handling. With it, for example, we are able to identify and select verbal data; to alphabetize; to sort, merge, and list various groups of words.

Unfortunately, this extraordinary ability of digital computers is sometimes misunderstood and gives rise to the fanciful notion that they are endowed with near-human or even superhuman qualities. Computer people encourage this in their vocabulary: You "instruct" and "query" the machine in its own "language"; it "accepts," "differentiates," "searches its memory," "analyzes," and even "evaluates." This anthropomorphizing creates an aura of mystery about computers and seduces people into believing that the machines can "think."

It is true that man has evolved ways to make the digital computer perform alpha-

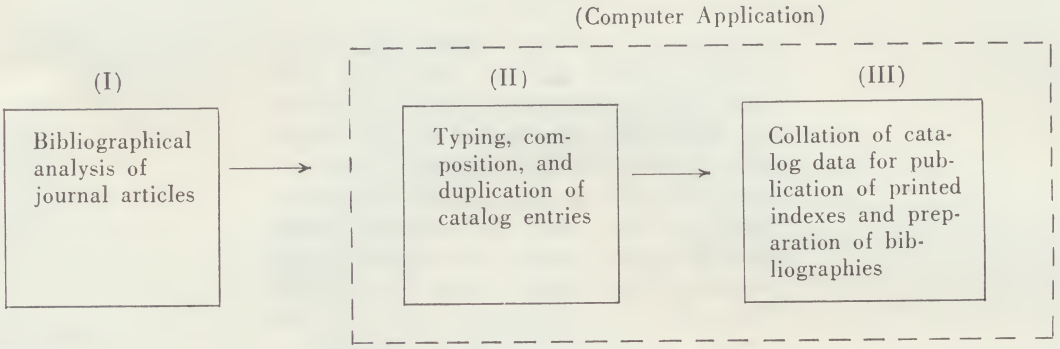


Fig. I—Routine Flow of Work

digital computer—hence the term "machine language." Production of machine language according to specifications is by far the most critical phase of the processing operation.

The final step in the conversion process occurs when the punched paper tapes are spliced together and run through a machine that transfers their intelligence to magnetic tape. The transfer procedure is quite simple—the holes in the punched paper tape are sensed and then faithfully duplicated as electrically charged spots on a spool of magnetic tape; MEDLARS input data are now ready for the computer.

The work the computer performs

A series of programs was written for MEDLARS that enables the computer to perform automatically many clerical operations previously done manually. For example, it can compare applied subject headings with a MESH authority file stored in memory to detect an invalid entry. It can generate full citations and assemble them as cross references in a master file. It can look for logical errors in the citations themselves and print out precisely where these occur. It can sort selected citations into alphabetic sequence. It can search its files to select information by any combination of elements which are contained in each citation, etc. Additional special computer programs also exist for processing requests for bibliographies and for generating lists of citations for eventual printing.

A unique machine called GRACE (Graphic Arts Composing Equipment) has been designed especially for MEDLARS; it is used peripherally to the main computer. This machine is capable of producing a positive film transparency ready for photo-offset printing.

GRACE is a one-of-a-kind machine for automatic electronic photo composition. Machines like it have existed for several years and are in common use for the automatic typesetting of newspaper advertisements. The advanced features of GRACE are its speed—30 times faster than predecessor machines—and its ability to utilize multiple type fonts to satisfy NLM's printing specifications.

In preparing the *Index Medicus* or the *Cumulative Index Medicus* for publication, the computer program first selects appropriate citations from its master file. Each citation contains the machine-language codes that are needed to make GRACE work. The program then organizes these citations into the order prescribed for publishing. All this results in output from the computer of a spool of magnetic tape containing the ultimate publication content and the instruction codes to operate GRACE. The output tape drives GRACE to produce automatically a positive film transparency. Citations on the film are properly justified, are grouped under their required subject headings, and appear in the various type fonts and sizes required to meet NLM's high-quality printing standards.

Many years of painstaking human effort on the part of the NLM professional library staff and their contractor, the General Electric Company, were required to conceive, design, and implement MEDLARS. Investigations first began in late 1960. This led to a preliminary design phase in late 1961 that took MEDLARS out of the concept stage and into the road-map stage essential for the detailed design phase that was to follow. The detailed design effort, begun in February 1962, lasted more than a year. During this time detailed performance specifications were prepared and

computer programs were written. The arrival of the computer did not occur until 1963 when a Honeywell 800 computer was installed and MEDLARS experienced its first shakedown. At this point NLM attempted to identify and exterminate as many of the conspicuous "bugs" as they could find. Several months later the manual system was replaced by the computer-driven system, except for GRACE. When GRACE is delivered in early 1964 total systems implementation will be completed.

MEDLARS objectives

Some librarians argue that MEDLARS constitutes an elaborate and expensive means of doing a job that traditionally has been done manually. On the other hand, others commend NLM for undertaking such pioneer work and view the effort as an important bench mark toward the achievement of more advanced goals. The following summarization of MEDLARS' objectives is to indicate whether the accomplishment of these objectives (which appears reasonably certain at this writing) will be worth the effort.

- Improve and enlarge *Index Medicus* and reduce the time required to prepare the monthly edition for printing from twenty-two to five working days.
- Produce other compilations similar to *Index Medicus* in form and content.
- Include citations derived from sources other than journal articles.
- Promptly (a maximum of two days) and efficiently service requests for special bibliographies on both a demand and a recurring basis, regularly searching at least five years of stored computer files.
- Increase the average depth of indexing per article by a factor of five, i.e., ten headings versus two.
- Nearly double the number of articles that may be handled annually—from the current 140,000 to 250,000 in 1969.
- Reduce the need for duplicative total-literature screening operations.
- Keep statistics and perform analyses of its own operations in order to provide the information needed to monitor and improve system effectiveness.
- Permit future expansion to incorporate new and as yet not completely defined objectives (e.g., communication of data from NLM to remote locations). •••

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